

Interconnect Analysis and Synthesis



Suranaree University of Technology



31051000609632

Kuan Cheng
John Lillis
Shen Lin
Norman Chang

Contents

Preface	xi
Acknowledgments	xiii
1 Introduction	1
1.1 Overview	1
1.2 Book Organization	2
1.2.1 Models and Analysis	3
1.2.2 Synthesis	3
2 Interconnect Models	5
2.1 Technology Trends	5
2.2 Device and Interconnect Scaling	6
2.2.1 Timing	8
2.2.2 Noise	8
2.2.3 Power	9
2.2.4 Reliability	9
2.3 Interconnect Models	10
2.3.1 Resistors	10
2.3.2 Capacitors	11
2.3.3 Inductors	12
2.3.4 RC Model	13
2.3.5 RLC Model	16

2.4	The Effect of Capacitive Coupling	22
2.4.1	Output Response of Step Input	23
2.4.2	Output Response of Ramp Input	29
2.5	The Effect of Inductive Coupling	30
2.6	Transmission Line Model	33
2.7	Power Dissipation	34
2.8	Interconnect Reliability	34
3	Device Models	39
3.1	Introduction	39
3.2	Device I - V Characteristics	39
3.3	General Format of Device Models	41
3.4	Device Models in Explicit Expression	42
3.5	Device Model Using a Table-Lookup Model	43
3.6	Effective Capacitance Model	45
4	Interconnect Analysis	51
4.1	Introduction	51
4.2	Time Domain Analysis	52
4.2.1	RLC Network Analysis	52
4.2.2	RC Network Analysis	54
4.2.3	Properties of the Matrices	55
4.2.4	Responses in Time Domain	56
4.3	S Domain Analysis	56
4.4	Circuit Reduction via Matrix Approximation	59
4.4.1	Stability and Passivity	65
4.5	Analysis Using Moment Matching	68
4.5.1	Concept of Moments	69
4.5.2	Delay Estimation Using Central Moments	70
4.5.3	Padé Approximation	72
4.5.4	Moment Derivation Using Interconnect Tree	76
4.5.5	Connection between Padé Approximation and PVL Matrix Approximation	78
4.5.6	Voltage-Time Area of RLC and RC Network	79
4.5.7	Capacitive Coupling Output with Respect to Ramp Input	80
4.5.8	Elmore Model (First-Order Moment) Analysis for Single Tree	81
4.5.9	Layout-Driven Analysis Procedure	83
4.5.10	Output π Model for RC Tree Reduction	84

4.6	Transmission Lines	85
4.6.1	Step Input Response	87
4.6.2	Attenuation, Phase Shift, and Characteristic Impedance	91
4.6.3	Reflected and Transmitted Waves	94
5	Inductance and Inductive Coupling for On-Chip Interconnect	99
5.1	Introduction	99
5.1.1	Differences in On-Chip Inductance Consideration	101
5.1.2	Spectrum and Significant Frequency of High-Speed Pulse	105
5.1.3	Inductance Calculation	108
5.1.4	Skin-Effect and Proximity-Effect Resistance Calculation	116
5.2	On-Chip Inductance Consideration	125
5.2.1	Handling Frequency-Dependent Resistance and Inductance	125
5.2.2	Worst Case and Inductance Impact on Delay and Crosstalk	129
5.2.3	When Do We Need to Consider On-Chip Inductance?	139
5.3	On-Chip Design Solutions to Cope with Inductance Effects	145
5.3.1	Dedicated Ground Wires	145
5.3.2	Differential Signals	146
5.3.3	Buffer Insertion	147
5.3.4	Splitting Wires	149
5.3.5	Terminations	153
5.3.6	Continuous Power/Ground Planes	156
5.4	Summary	157
6	Synthesis: Overview and Static Topology Optimization	161
6.1	Introduction	161
6.2	Overview of Interconnect Synthesis	162
6.2.1	Delay Estimators	162
6.2.2	Design Space	164
6.2.3	Problem Formulations	166
6.2.4	Scaling Coefficients	168
6.2.5	Error in Delay Estimators	169
6.3	Optimization of Static Routing Topologies	170
6.3.1	Notational Conventions	170
6.3.2	Formulations	171

6.3.3	Algorithmic Framework	172
6.3.4	Maximizing Required Arrival Time	173
6.3.5	Minimizing Total Capacitance Subject to Timing Constraints	178
6.3.6	Accounting for Signal Slew	183
6.4	Summary, Discussion, and Further Reading	189
6.5	Exercises	190
7	Global Routing Topology Synthesis	193
7.1	Introduction	193
7.2	Background and Overview	193
7.2.1	Algorithm Overview	193
7.3	Preliminaries	196
7.3.1	Delay Models	196
7.3.2	Graphs, Trees, and Permutations	197
7.4	Finding High-Quality Sink Permutations	199
7.4.1	Hierarchy Construction and Reorientation	199
7.4.2	Tour Length Minimization	200
7.5	Tree Construction for a Given Permutation	202
7.5.1	Overview	202
7.5.2	Routing for Min-Area: The P-Tree _A Algorithm	204
7.5.3	Routing for Performance: The P-Tree _{AT} Algorithm	206
7.5.4	Complexity	209
7.5.5	Heuristic Limitation of cq-Set Size	211
7.6	Experiments	211
7.7	Summary and Comments	216
7.7.1	Speedup Techniques and P-Tree-like Algorithms	217
7.7.2	Delay Model Generalizations	219
7.8	Further Reading	219
7.9	Exercises	220
8	Optimization of Multisource Nets	223
8.1	Introduction	223
8.2	Preliminaries and Formulations	225
8.3	Linear Time Computation of $ARD(T)$ Under Elmore	227
8.4	The Repeater Insertion Algorithm	229
8.4.1	A Motivational Example	230
8.4.2	Solution Characterization	232
8.4.3	PWL Primitives	232

8.4.4	Solution Dominance	233
8.4.5	The Overall Algorithm	235
8.4.6	Discussion	238
8.5	Summary, Discussion, and Further Reading	238
8.6	Exercises	239
9	Timing-Driven Maze Routing	241
9.1	Introduction	241
9.2	Assumptions	242
9.3	Formulations	243
9.4	Algorithms	245
9.4.1	Dominance	245
9.4.2	A Sink-to-source Algorithm for Bufferless Constrained Maze Routing	245
9.5	A Label-Setting Refinement	247
9.6	Example	248
9.7	An Algorithm for Formulation 9.2	252
9.8	Incorporating Buffer Insertion	253
9.9	Complexity	254
9.10	Summary and Comments	255
9.11	Exercises	257
	Index	259