



# EMBEDDED SYSTEMS AND SOFTWARE VALIDATION

ABHIK ROYCHOUDHURY

SYSTEMS  
ON  
SILICON



M K®  
MORGAN KAUFMANN

# Contents

Acknowledgments .....	ix	
Preface .....	xi	
<b>CHAPTER 1</b>	<b>Introduction</b>	<b>1</b>
<b>CHAPTER 2</b>	<b>Model Validation</b>	<b>7</b>
<b>2.1</b>	Platform versus System Behavior .....	8
<b>2.2</b>	Criteria for Design Model.....	10
<b>2.3</b>	Informal Requirements: A Case Study .....	12
2.3.1	The Requirements Document .....	13
2.3.2	Simplification of the Informal Requirements .....	14
<b>2.4</b>	Common Modeling Notations .....	16
2.4.1	Finite-State Machines .....	16
2.4.2	Communicating FSMs .....	20
2.4.3	Message Sequence Chart-Based Models .....	27
<b>2.5</b>	Remarks about Modeling Notations .....	37
<b>2.6</b>	Model Simulations .....	39
2.6.1	FSM Simulations .....	41
2.6.2	Simulating MSC-Based System Models .....	46
<b>2.7</b>	Model-Based Testing .....	50
<b>2.8</b>	Model Checking .....	58
2.8.1	Property Specification .....	58
2.8.2	Checking Procedure .....	73
<b>2.9</b>	The SPIN Validation Tool .....	82
<b>2.10</b>	The SMV Validation Tool .....	86
<b>2.11</b>	Case Study: Air-Traffic Controller.....	89
<b>2.12</b>	References .....	91
<b>2.13</b>	Exercises .....	93
<b>CHAPTER 3</b>	<b>Communication Validation</b>	<b>95</b>
<b>3.1</b>	Common Incompatibilities .....	98
3.1.1	Sending/Receiving Signals in Different Order.....	99
3.1.2	Handling a Different Signal Alphabet .....	100
3.1.3	Mismatch in Data Format .....	102
3.1.4	Mismatch in Data Rates .....	105
<b>3.2</b>	Converter Synthesis .....	106
3.2.1	Representing Native Protocols and Converters .....	106
3.2.2	Basic Ideas for Converter Synthesis .....	108
3.2.3	Various Strategies for Protocol Conversion .....	115

3.2.4	Avoiding No-Progress Cycles.....	116
3.2.5	Speculative Transmission to Avoid Deadlocks.....	118
<b>3.3</b>	Changing a Working Design .....	121
<b>3.4</b>	References .....	122
<b>3.5</b>	Exercises .....	123
<b>CHAPTER 4 Performance Validation</b>		<b>125</b>
<b>4.1</b>	The Conventional Abstraction of Time .....	126
<b>4.2</b>	Predicting Execution Time of a Program.....	131
4.2.1	WCET Calculation .....	133
4.2.2	Modeling of Microarchitecture .....	145
<b>4.3</b>	Interference within a Processing Element.....	154
4.3.1	Interrupts from Environment .....	155
4.3.2	Contention and Preemption .....	157
4.3.3	Sharing a Processor Cache .....	161
<b>4.4</b>	System-Level Communication Analysis .....	165
<b>4.5</b>	Designing Systems with Predictable Timing.....	169
4.5.1	Scratchpad Memories .....	169
4.5.2	Time-Triggered Communication .....	174
<b>4.6</b>	Emerging Applications .....	176
<b>4.7</b>	References .....	177
<b>4.8</b>	Exercises .....	177
<b>CHAPTER 5 Functionality Validation</b>		<b>181</b>
<b>5.1</b>	Dynamic or Trace-Based Checking .....	184
5.1.1	Dynamic Slicing .....	187
5.1.2	Fault Localization .....	196
5.1.3	Directed Testing Methods .....	203
<b>5.2</b>	Formal Verification .....	207
5.2.1	Predicate Abstraction .....	211
5.2.2	Software Checking via Predicate Abstraction.....	218
5.2.3	Combining Formal Verification with Testing .....	225
<b>5.3</b>	References .....	229
<b>5.4</b>	Exercises .....	230
<b>Bibliography</b>		<b>233</b>
<b>Index</b>		<b>241</b>