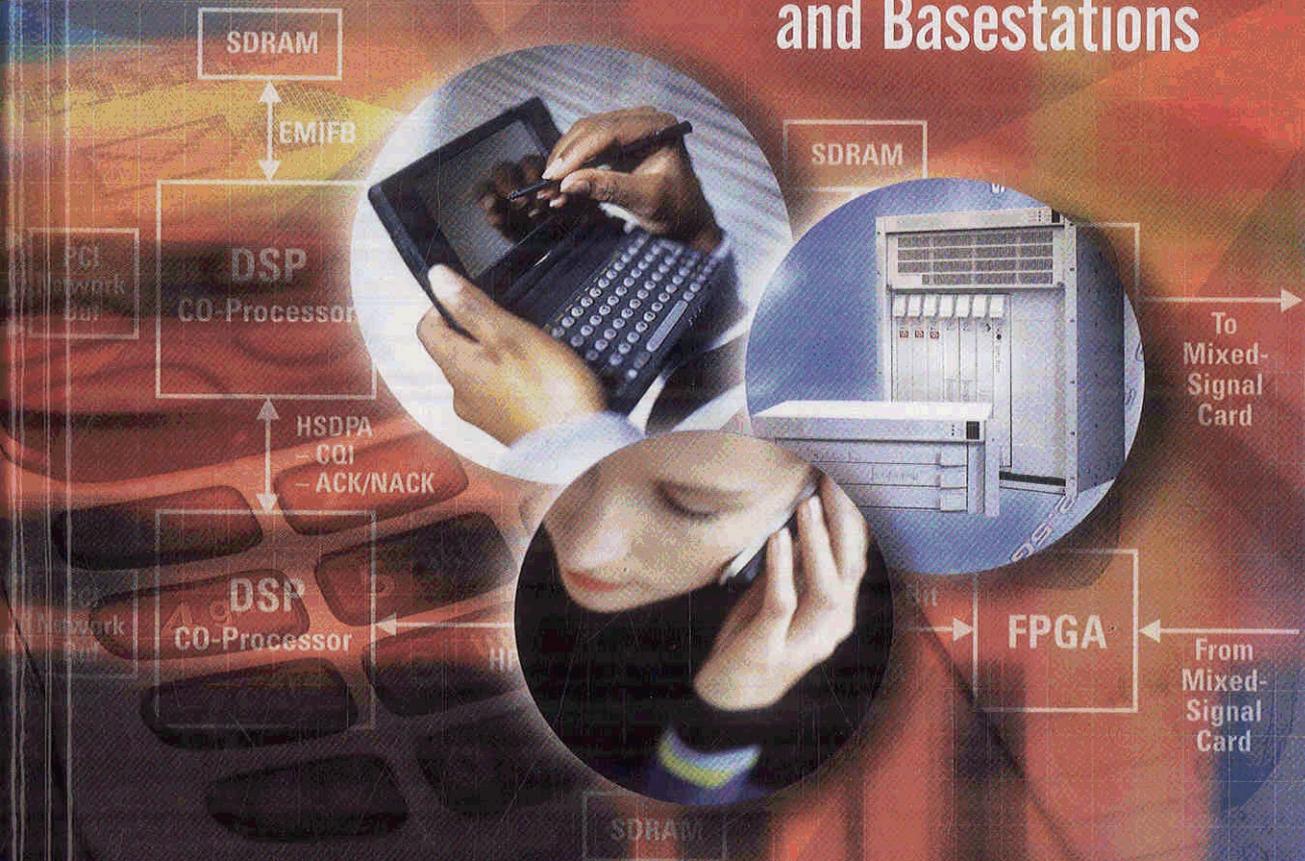


# software defined radio

## Baseband Technology for 3G Handsets and Basestations



Edited by **Walter Tuttlebee**

# Contents

<b>List of Contributors</b>	xv
<b>Foreword</b> <i>Stephen M. Blust</i>	xix
<b>Abbreviations</b>	xxi
<b>Biographies</b>	xxix
<b>Introduction</b> <i>Walter Tuttlebee</i>	1
<b>Part I: Requirements</b>	5
<b>1 SDR Baseband Requirements and Directions to Solutions</b>	7
<i>Mark Cummings</i>	
1.1. Baseband Technology and the Emergence of SDR	7
1.1.1. <i>Wireless Architectures</i>	7
1.1.2. <i>The Impact of Digital Technology</i>	9
1.1.3. <i>Growth of the Wireless Markets and Multiple Standards</i>	10
1.2. Evolution of SDR Baseband Requirements	12
1.2.1. <i>System Optimization</i>	12
1.2.2. <i>Market Drivers of SDR</i>	12
1.2.3. <i>Technology Drivers of SDR</i>	13
1.2.4. <i>Requirements by Application Environment</i>	14
1.3. Mobile End-user Systems	15
1.3.1. <i>Simple Handsets</i>	15
1.3.2. <i>Converged Devices</i>	18
1.3.3. <i>Notebooks</i>	19
1.3.4. <i>Vehicular Systems</i>	20
1.4. Fixed End-User Systems	22
1.4.1. <i>Infrastructure System Requirements</i>	22
1.4.2. <i>Basestation Requirements</i>	23

1.5.	Today's SDR Baseband Technology Approaches	24
1.5.1.	<i>Technologies and Criteria</i>	24
1.5.2.	<i>Capabilities and Constraints</i>	25
1.5.3.	<i>A Way Forward?</i>	27
1.6.	Conclusions	28
	Acknowledgments	29
	References	29
<b>Part II: Handset Technologies</b>		<b>31</b>
<b>2</b>	<b>Open Mobile Handset Architectures Based on the ZSP500 Embedded DSP Core</b>	<b>33</b>
<i>Jitendra Rayala and Wei-Jei Song</i>		
2.1.	Introduction	33
2.2.	Handset Requirements	34
2.2.1.	<i>Flexibility/Multifunctionality</i>	34
2.2.2.	<i>Multimode/Adaptive Modulation</i>	35
2.2.3.	<i>Scalability/Modularity</i>	35
2.2.4.	<i>Power Efficiency</i>	35
2.2.5.	<i>Algorithm Support</i>	35
2.3.	An Open Mobile Handset Architecture	39
2.3.1.	<i>The ZSP500 DSP Core</i>	40
2.3.2.	<i>The Role and Use of Coprocessors</i>	45
2.3.3.	<i>Development Tools for SoC design</i>	47
2.4.	Summary	48
	Acknowledgments	49
	References	49
<b>3</b>	<b>DSP for Handsets: The Blackfin Processor</b>	<b>51</b>
<i>Jose Fridman and Zoran Zvonar</i>		
3.1.	Handsets and the Progress of SDR	51
3.1.1.	<i>The Appeal of SDR</i>	51
3.1.2.	<i>Multistandard Terminals</i>	52
3.1.3.	<i>Wireless Handset Architecture – The Baseband Platform</i>	53
3.2.	The Blackfin Core	54
3.2.1.	<i>Key Features</i>	55
3.2.2.	<i>The Blackfin DSP Architecture</i>	55
3.2.3.	<i>Instruction Set</i>	57
3.2.4.	<i>Arithmetic Data Path and Programming Model</i>	57
3.2.5.	<i>Memory Architecture</i>	59
3.2.6.	<i>Operating Modes</i>	60
3.2.7.	<i>Interrupt System</i>	60
3.2.8.	<i>Debug Features</i>	61
3.2.9.	<i>Implementation Using the Blackfin Core</i>	61

3.3.	Handset Application Examples and Benchmarks	63
3.3.1.	<i>Finite Impulse Response Filter</i>	63
3.3.2.	<i>Viterbi Algorithm</i>	63
3.3.3.	<i>Motion Estimation</i>	65
3.3.4.	<i>Performance Benchmarks</i>	67
3.4.	The SoftFone Digital Baseband Architecture	68
3.4.1.	<i>SDR-related Features</i>	69
3.4.2.	<i>The AD6532 DBB Platform</i>	70
3.4.3.	<i>Architectural Extensions for Multimode Operation</i>	72
3.5.	Conclusions	72
	Acknowledgments	72
	References	73
<b>4</b>	<b>XPP – An Enabling Technology for SDR Handsets</b>	<b>75</b>
	<i>Eberhard Schüler and Lorna Tan</i>	
4.1.	Introduction	75
4.1.1.	<i>The Challenge</i>	75
4.1.2.	<i>The Dilemma</i>	75
4.1.3.	<i>Partitioning a System</i>	76
4.2.	The XPP Reconfigurable Processor	78
4.2.1.	<i>The XPP Basic Concepts</i>	78
4.2.2.	<i>The Processing Array</i>	80
4.2.3.	<i>Packets, Streams and Synchronization</i>	83
4.2.4.	<i>Reconfiguration Management</i>	85
4.2.5.	<i>Power Management</i>	86
4.2.6.	<i>Development Tools</i>	86
4.3.	Examples for Baseband Processing	89
4.3.1.	<i>W-CDMA/CDMA Receiver</i>	89
4.3.2.	<i>OFDM Decoder</i>	93
4.4.	Software Defined Radio Processor SDRXPP	96
4.4.1.	<i>Structure</i>	96
4.4.2.	<i>Processor Extensions for Baseband Processing</i>	97
4.5.	Conclusions	97
	Acknowledgments	98
	References	98
	Bibliography	98
<b>5</b>	<b>Adaptive Computing as the Enabling Technology for SDR</b>	<b>99</b>
	<i>David Chou, Jun Han, Jasmin Oz, Sharad Sambhwani and Cameron Stevens</i>	
5.1.	Introduction	99
5.2.	Algorithmic Evaluations in Communications	100
5.2.1.	<i>Algorithmic Subsets</i>	100
5.2.2.	<i>Algorithm Space</i>	101
5.2.3.	<i>The True Nature of Algorithms</i>	101

5.2.4.	<i>Classification of Algorithms</i>	103
5.2.5.	<i>The IC Gold Standard</i>	104
5.3.	Solving P <sup>3</sup> – Performance, Power Consumption and Price	104
5.3.1.	<i>Today's Design Issues</i>	104
5.3.2.	<i>Field Programmable Gate Arrays (FPGAs)</i>	105
5.3.3.	<i>Heterogeneous Processors for Heterogeneous Algorithms</i>	106
5.3.4.	<i>Node Types and Features</i>	107
5.3.5.	<i>Homogeneous Infrastructure</i>	108
5.3.6.	<i>Scalability</i>	108
5.3.7.	<i>Real-time Adaptability</i>	108
5.4.	Design Advantages	109
5.4.1.	<i>Solving Hardware/Software Codesign</i>	109
5.4.2.	<i>The SilverC Language</i>	109
5.4.3.	<i>Specifying the Computation</i>	113
5.4.4.	<i>Writing to Output Pipes</i>	114
5.4.5.	<i>Pipe Synchronization</i>	114
5.4.6.	<i>Instantiating Modules</i>	114
5.4.7.	<i>Linking Modules</i>	115
5.4.8.	<i>Constraining Modules</i>	115
5.4.9.	<i>SilverC Support for Spatial and Temporal Extensions</i>	115
5.5.	ACM Benchmarks	116
5.5.1.	<i>General Benchmarks</i>	116
5.5.2.	<i>W-CDMA Baseband Transceiver Benchmarks</i>	119
5.6.	Marketplace Benefits	127
5.7.	Technology Status	128
	References	128
<b>6</b>	<b>The Sandbridge Sandblaster Communications Processor</b>	<b>129</b>
	<i>John Glossner, Erdem Hokenek and Mayan Moudgill</i>	
6.1.	Rationale for SDR Processors	129
6.1.1.	<i>The Challenge</i>	130
6.1.2.	<i>Tiers of Software Radio</i>	130
6.1.3.	<i>The Benefits</i>	131
6.2.	Processor Architecture	131
6.2.1.	<i>Definitions and Architecture Evolution</i>	131
6.2.2.	<i>Microarchitecture</i>	133
6.2.3.	<i>Token Triggered Multithreading</i>	138
6.2.4.	<i>Compound Instructions</i>	139
6.2.5.	<i>Processing Datatypes</i>	140
6.2.6.	<i>Interrupts</i>	140
6.2.7.	<i>Synchronization</i>	140
6.2.8.	<i>Java Support</i>	140
6.3.	Processor Software Tools	141
6.3.1.	<i>Compilers</i>	141
6.3.2.	<i>Performance Simulation</i>	144

6.3.3. <i>The Integrated Development Environment (IDE)</i>	151
6.3.4. <i>The Real-Time Operating System (RTOS)</i>	151
6.4. A 3G System SDR Implementation	153
6.4.1. <i>The Conventional Multiple Processor Approach</i>	153
6.4.2. <i>The SDR Convergence Processor Approach</i>	153
6.4.3. <i>The UMTS WCDMA FDD Requirement</i>	153
6.4.4. <i>3G SDR Implementation and Performance</i>	155
6.5. Conclusions	156
References	157

### **Part III: Basestation Technologies** **161**

#### **7 Cost Effective Software Radio for CDMA Systems** **163**

*Alan Gatherer, Sundararajan Sriram, Filip Moerman,  
Chaitali Sengupta and Kathy Brown*

7.1. Introduction	163
7.1.1. <i>The Phases of Baseband Development</i>	163
7.1.2. <i>Software Radio and Technology Intercept</i>	163
7.1.3. <i>Technology Intercept versus Time</i>	164
7.1.4. <i>Evolution from Today's Basestation Technology</i>	164
7.1.5. <i>Chapter Structure</i>	165
7.2. Today's Software/Hardware Trade-off in WCDMA Modems	166
7.2.1. <i>Hardware Implemented Elements</i>	166
7.2.2. <i>Software Implemented Elements</i>	167
7.2.3. <i>The 'Debatable' Functionality</i>	167
7.3. Temporal Processing Domains	167
7.3.1. <i>Temporal Domains in WCDMA</i>	167
7.3.2. <i>Partitioning Implications</i>	167
7.4. The Evolution of Chip-Rate Processing	168
7.4.1. <i>The Key Challenge</i>	168
7.4.2. <i>Evolutionary Approaches</i>	169
7.4.3. <i>Today's Solution</i>	170
7.5. The Importance of Efficient Interfaces to Minimize Overhead	170
7.5.1. <i>Coprocessor Data Exchange</i>	171
7.5.2. <i>Interface Requirements</i>	171
7.5.3. <i>Programmable Interface Configuration</i>	171
7.6. Real Time Processing on a Programmable Device	172
7.6.1. <i>Sub-slot Latency Demands</i>	172
7.6.2. <i>Downlink Power Control Processing</i>	172
7.6.3. <i>Overcoming the Software Bottleneck</i>	174
7.7. The TCI Platform	175
7.8. Summary	176
References	176

<b>8 DSP for Basestations – The TigerSHARC</b>	<b>177</b>
<i>Michael J. Lopez, Rasekh Rifaat and Qian Zhang</i>	
8.1. Introduction and Philosophy	177
8.2. Device Architecture	179
8.2.1. Highlights	179
8.2.2. SDR Features of the Device	181
8.3. Special Instructions for Communications Signal Processing	183
8.3.1. Chip-Rate Processing in 3G Cellular Baseband	183
8.3.2. Channel Decoding and Equalization	187
8.4. System Design	190
8.4.1. CDMA System Load Balancing	190
8.4.2. Scheduling	192
8.4.3. Pre-despreading versus Frame Buffering	192
8.4.4. Processing Distribution Across Multiple DSPs	194
8.5. Advanced Receiver Techniques	195
8.5.1. Multi-User Detection (MUD)	195
8.5.2. Smart Antennas	199
8.6. Summary	200
Acknowledgments	200
References	200
<b>9 Altera System Architecture Solutions for SDR</b>	<b>203</b>
<i>Paul Ekas</i>	
9.1. Setting the Scene	203
9.1.1. Cellular Baseband SDR Requirements	203
9.1.2. FPGAs are Not What They Were	204
9.2. SDR Design Choices	205
9.2.1. SDR Conceptual Architecture – Dynamic Functions	205
9.2.2. Mapping to an Implementation Architecture – System Partitioning	207
9.2.3. Software/Hardware Partitioning	208
9.3. The Future of FPGAs	211
9.3.1. What is an FPGA?	211
9.3.2. Fabric of Logic Elements with General and DSP Arrays	212
9.3.3. Three Representative FPGA System Partitionings	214
9.4. Architectural Solutions	216
9.4.1. The Baseband SDR Design Process	217
9.4.2. Device Families	220
9.4.3. Intellectual Property Availability	221
9.5. Design Flow and Tools	223
9.5.1. Importance of Tools	223
9.5.2. System-Level Design Products with Quartus II	223
9.5.3. Quartus II Design Software	225

9.6. Representative Devices	226
9.6.1. <i>Stratix</i>	226
9.6.2. <i>Stratix GX</i>	227
9.6.3. <i>Excalibur</i>	229
9.6.4. <i>Cyclone</i>	231
9.7. Conclusions	233
9.7.1. <i>Current Confirmation</i>	233
9.7.2. <i>Inevitable Evolution</i>	233
References	233

## **10 FPGAs: A Platform-Based Approach to Software Radios** **235**

*Chris Dick and Jim Hwang*

10.1. The FPGA as Signal Processor	235
10.1.1. <i>Semiconductor Trends</i>	235
10.1.2. <i>Computing Architectures</i>	236
10.1.3. <i>Architectural Customization</i>	236
10.2. Designing for the Architecture	239
10.2.1. <i>Appropriate Architecture allows Silicon Efficiency</i>	241
10.3. A New Approach to FPGA Programming	242
10.3.1. <i>The Complexity of Traditional FPGA Design</i>	242
10.3.2. <i>New FPGA Design Flows</i>	243
10.3.3. <i>Programming Custom Hardware</i>	243
10.3.4. <i>Programming for FPGAs</i>	244
10.3.5. <i>System Generator for DSP</i>	245
10.3.6. <i>Interaction with Matlab</i>	246
10.3.7. <i>Programmatic Customization using M-Code</i>	247
10.3.8. <i>Co-simulation Interfaces</i>	250
10.3.9. <i>Embedded Systems</i>	251
10.4. FPGA DSP Usage in the Radio PHY	251
10.4.1. <i>Case Study – Digital Down Conversion</i>	252
10.4.2. <i>Case Study – MultiChannel Receiver</i>	258
10.4.3. <i>Case Study – Adaptive Systems</i>	264
10.5. Conclusion	268
10.5.1. <i>New Century, New Requirements</i>	268
10.5.2. <i>Increasing Demands for Reprogrammability</i>	268
10.5.3. <i>Future Requirements and Solutions</i>	269
References	270

## **11 Reconfigurable Parallel DSP – rDSP** **273**

*Behzad Mohebbi and Fadi J. Kurdahi*

11.1. Introduction	273
11.1.1. <i>Types of Parallel Architecture</i>	274
11.1.2. <i>Reconfigurable Architectures</i>	274

11.2.	Baseband Algorithms and Parallelism	274
11.2.1.	<i>Source Encoder/Decoder</i>	277
11.2.2.	<i>Encryption Encoder/Decoder</i>	279
11.2.3.	<i>FEC Encoder/Decoder</i>	280
11.2.4.	<i>Interleaver/Deinterleaver</i>	282
11.2.5.	<i>Modulation/Demodulation</i>	283
11.2.6.	<i>Interpolation and Pulse-Shaping Filtering</i>	285
11.2.7.	<i>Inner Receiver</i>	285
11.2.8.	<i>Summary</i>	288
11.3.	The MS1 Reconfigurable DSP (rDSP)	289
11.3.1.	<i>The MS1 rDSP Architecture</i>	289
11.3.2.	<i>Development Tools for the MS1 rDSP</i>	291
11.4.	Implementing a 3G Air Interface in SDR	292
11.4.1.	<i>The WCDMA AMR Channel</i>	293
11.4.2.	<i>Transmitter and Propagation Channel</i>	293
11.4.3.	<i>A Software-Defined Receiver Implementation</i>	295
11.4.4.	<i>Performance Capability</i>	298
11.5.	Conclusion	300
	Acknowledgments	300
	References	300

## **12 The picoArray: A Reconfigurable SDR Processor for Basestations** **303**

*Rupert Baines*

12.1.	Introduction	304
12.1.1.	<i>Shannon, Moore and the Design Gap</i>	304
12.1.2.	<i>The Drivers for Flexibility</i>	304
12.2.	The 3G Design Challenge	305
12.2.1.	<i>The Challenge of 3G WCDMA Basestations</i>	305
12.2.2.	<i>Increasing Complexity Demands</i>	307
12.2.3.	<i>Conventional Architectures</i>	307
12.3.	Reconfigurable Architectures	311
12.3.1.	<i>A Variety of Approaches</i>	311
12.3.2.	<i>Reconfigurability and 'Reconfigurability'</i>	312
12.3.3.	<i>The Parallel Processor Array</i>	313
12.3.4.	<i>Problems with Parallelism</i>	313
12.3.5.	<i>The picoArray</i>	313
12.3.6.	<i>A Common Processing Environment</i>	316
12.3.7.	<i>Control and Data</i>	316
12.3.8.	<i>Programming and Verification</i>	317
12.3.9.	<i>Control and Management</i>	320
12.4.	Comparison of Different Approaches	320
12.4.1.	<i>Simple Performance Metrics</i>	320
12.4.2.	<i>Benchmarks</i>	322

Contents	xiii
<hr/>	
12.5. A Commercial 3G Node B Implementation	326
12.5.1. System Implementation	326
12.5.2. Total Cost of Ownership	326
12.6. Other Applications for the picoArray	328
12.7. Summary	329
References	330
<b>Part IV: Epilogue: Strategic Impact</b>	<b>331</b>
<b>13 The Impact of Technological Change</b>	<b>333</b>
<i>Walter Tuttlebee</i>	
13.1. New Technology	333
13.1.1. Perspectives	333
13.1.2. The Technology S-curve	334
13.1.3. Technology Drivers and Trends	336
13.1.4. A Technology Taxonomy	337
13.2. Industry Impact	338
13.2.1. Multi-Standard Phones	338
13.2.2. On-the-fly Terminal Reconfiguration	339
13.2.3. Basestations	339
13.2.4. The Wider Electronics Industry	340
13.3. Concluding Remarks	340
Acknowledgements	341
References	341
<b>Index</b>	<b>343</b>