

# CONTENTS

<b>PREFACE TO THE SECOND EDITION</b>	<b>xix</b>
<b>PART 1 DESIGN TECHNOLOGIES AND SKILLS</b>	<b>1</b>
<b>1 DIFFERENCE BETWEEN RF AND DIGITAL CIRCUIT DESIGN</b>	<b>3</b>
1.1 Controversy	3
1.1.1 Impedance Matching	4
1.1.2 Key Parameter	5
1.1.3 Circuit Testing and Main Test Equipment	6
1.2 Difference of RF and Digital Block in a Communication System	6
1.2.1 Impedance	6
1.2.2 Current Drain	7
1.2.3 Location	7
1.3 Conclusions	9
1.4 Notes for High-Speed Digital Circuit Design	9
Further Reading	10
Exercises	11
Answers	11
<b>2 REFLECTION AND SELF-INTERFERENCE</b>	<b>15</b>
2.1 Introduction	15
2.2 Voltage Delivered from a Source to a Load	16
2.2.1 General Expression of Voltage Delivered from a Source to a Load when $l \ll \lambda/4$ so that $T_d \rightarrow 0$	16
2.2.2 Additional Jitter or Distortion in a Digital Circuit Block	20
2.3 Power Delivered from a Source to a Load	23
2.3.1 General Expression of Power Delivered from a Source to a Load when $l \ll \lambda/4$ so that $T_d \rightarrow 0$	23
2.3.2 Power Instability	26
2.3.3 Additional Power Loss	27
2.3.4 Additional Distortion	28
2.3.5 Additional Interference	31
2.4 Impedance Conjugate Matching	33
2.4.1 Maximizing Power Transport	33
2.4.2 Power Transport without Phase Shift	35

2.4.3	Impedance Matching Network	37
2.4.4	Necessity of Impedance Matching	40
2.5	Additional Effect of Impedance Matching	42
2.5.1	Voltage Pumped up by Means of Impedance Matching	42
2.5.2	Power Measurement	49
Appendices		51
2.A.1	VSWR and Other Reflection and Transmission Coefficients	51
2.A.2	Relationships between Power ( $\text{dB}_m$ ), Voltage (V), and Power (W)	58
Reference		58
Further Reading		58
Exercises		59
Answers		59
<b>3</b>	<b>IMPEDANCE MATCHING IN THE NARROW-BAND CASE</b>	<b>61</b>
3.1	Introduction	61
3.2	Impedance Matching by Means of Return Loss Adjustment	63
3.2.1	Return Loss Circles on the Smith Chart	63
3.2.2	Relationship between Return Loss and Impedance Matching	66
3.2.3	Implementation of an Impedance Matching Network	67
3.3	Impedance Matching Network Built by One Part	68
3.3.1	One Part Inserted into Impedance Matching Network in Series	68
3.3.2	One Part Inserted into the Impedance Matching Network in Parallel	70
3.4	Impedance Matching Network Built by Two Parts	74
3.4.1	Regions in a Smith Chart	74
3.4.2	Values of Parts	75
3.4.3	Selection of Topology	81
3.5	Impedance Matching Network Built By Three Parts	84
3.5.1	“ $\Pi$ ” Type and “T” Type Topologies	84
3.5.2	Recommended Topology	84
3.6	Impedance Matching When $Z_S$ Or $Z_L$ Is Not $50 \Omega$	85
3.7	Parts In An Impedance Matching Network	93
Appendices		94
3.A.1	Fundamentals of the Smith Chart	94
3.A.2	Formula for Two-Part Impedance Matching Network	99
3.A.3	Topology Limitations of the Two-Part Impedance Matching Network	110
3.A.4	Topology Limitation of Three Parts Impedance Matching Network	114
3.A.5	Conversion between $\Pi$ and T Type Matching Network	122
3.A.6	Possible $\Pi$ and T Impedance Matching Networks	124
Reference		124
Further Reading		124

## CONTENTS

Exercises	125
Answers	127
<b>4 IMPEDANCE MATCHING IN THE WIDEBAND CASE</b>	<b>131</b>
4.1 Appearance of Narrow and Wideband Return Loss on a Smith Chart	131
4.2 Impedance Variation Due to the Insertion of One Part Per Arm or Per Branch	136
4.2.1 An Inductor Inserted into Impedance Matching Network in Series	137
4.2.2 A Capacitor Inserted into Impedance Matching Network in Series	139
4.2.3 An Inductor Inserted into Impedance Matching Network in Parallel	141
4.2.4 A Capacitor Inserted into Impedance Matching Network in Parallel	143
4.3 Impedance Variation Due to the Insertion of Two Parts Per Arm or Per Branch	145
4.3.1 Two Parts Connected in Series to Form One Arm	146
4.3.2 Two Parts Are Connected in Parallel to Form One Branch	148
4.4 Partial Impedance Matching for an IQ (in Phase Quadrature) Modulator in a UWB (Ultra Wide Band) System	151
4.4.1 Gilbert Cell	151
4.4.2 Impedances of the Gilbert Cell	153
4.4.3 Impedance Matching for LO, RF, and IF Ports Ignoring the Bandwidth	155
4.4.4 Wide Bandwidth Required in a UWB (Ultra Wide Band) System	159
4.4.5 Basic Idea to Expand the Bandwidth	160
4.4.6 Example 1: Impedance Matching in IQ Modulator Design for Group 1 in a UWB System	161
4.4.7 Example 2: Impedance Matching in IQ Modulator Design for Group 3 + Group 6 in a UWB System	172
4.5 Discussion of Passive Wideband Impedance Matching Network	174
4.5.1 Impedance Matching for the Gate of a MOSFET Device	175
4.5.2 Impedance Matching for the Drain of a MOSFET Device	177
Further Reading	179
Exercises	179
Answers	180
<b>5 IMPEDANCE AND GAIN OF A RAW DEVICE</b>	<b>181</b>
5.1 Introduction	181
5.2 Miller Effect	183
5.3 Small-Signal Model of a Bipolar Transistor	187
5.4 Bipolar Transistor with CE (Common Emitter) Configuration	190
5.4.1 Open-Circuit Voltage Gain $A_{v,CE}$ of a CE Device	190

5.4.2	Short-Circuit Current Gain $\beta_{CE}$ and Frequency Response of a CE Device	194
5.4.3	Primary Input and Output Impedance of a CE (common emitter) device	196
5.4.4	Miller's Effect in a Bipolar Transistor with CE Configuration	197
5.4.5	Emitter Degeneration	200
5.5	Bipolar Transistor with CB (Common Base) Configuration	204
5.5.1	Open-Circuit Voltage Gain $A_{v,CB}$ of a CB Device	204
5.5.2	Short-Circuit Current Gain $\beta_{CG}$ and Frequency Response of a CB Device	206
5.5.3	Input and Output Impedance of a CB Device	208
5.6	Bipolar Transistor with CC (Common Collector) Configuration	214
5.6.1	Open-Circuit Voltage Gain $A_{v,CC}$ of a CC Device	214
5.6.2	Short-Circuit Current Gain $\beta_{CC}$ and Frequency Response of the Bipolar Transistor with CC Configuration	217
5.6.3	Input and Output Impedance of a CC Device	218
5.7	Small-Signal Model of a MOSFET	221
5.8	Similarity Between a Bipolar Transistor and a MOSFET	225
5.8.1	Simplified Model of CS Device	225
5.8.2	Simplified Model of CG Device	228
5.8.3	Simplified Model of CD Device	230
5.9	MOSFET with CS (Common Source) Configuration	235
5.9.1	Open-Circuit Voltage Gain $A_{v,CS}$ of a CS Device	235
5.9.2	Short-Circuit Current Gain $\beta_{CS}$ and Frequency Response of a CS Device	237
5.9.3	Input and Output Impedance of a CS Device	239
5.9.4	Source Degeneration	240
5.10	MOSFET with CG (Common Gate) Configuration	244
5.10.1	Open-Circuit Voltage Gain of a CG Device	244
5.10.2	Short-Circuit Current Gain and Frequency Response of a CG Device	245
5.10.3	Input and Output Impedance of a CG Device	247
5.11	MOSFET with CD (Common Drain) Configuration	249
5.11.1	Open-Circuit Voltage Gain $A_{v,CD}$ of a CD Device	250
5.11.2	Short-Circuit Current Gain $\beta_{CD}$ and Frequency Response of a CD Device	250
5.11.3	Input and Output Impedance of a CD Device	251
5.12	Comparison of Transistor Configuration of Single-stage Amplifiers with Different Configurations	252
	Further Reading	256
	Exercises	256
	Answers	256
<b>6</b>	<b>IMPEDANCE MEASUREMENT</b>	<b>259</b>
6.1	Introduction	259
6.2	Scalar and Vector Voltage Measurement	260

6.2.1	Voltage Measurement by Oscilloscope	260
6.2.2	Voltage Measurement by Vector Voltmeter	262
6.3	Direct Impedance Measurement by a Network Analyzer	263
6.3.1	Direction of Impedance Measurement	263
6.3.2	Advantage of Measuring $S$ Parameters	265
6.3.3	Theoretical Background of Impedance Measurement by $S$ Parameters	266
6.3.4	$S$ Parameter Measurement by Vector Voltmeter	268
6.3.5	Calibration of the Network Analyzer	270
6.4	Alternative Impedance Measurement by Network Analyzer	272
6.4.1	Accuracy of the Smith Chart	272
6.4.2	Low- and High-Impedance Measurement	275
6.5	Impedance Measurement Using a Circulator	276
	Appendices	277
6.A.1	Relationship Between the Impedance in Series and in Parallel	277
	Further Reading	278
	Exercises	278
	Answers	279
<b>7</b>	<b>GROUNDING</b>	<b>281</b>
7.1	Implication of Grounding	281
7.2	Possible Grounding Problems Hidden in a Schematic	283
7.3	Imperfect or Inappropriate Grounding Examples	284
7.3.1	Inappropriate Selection of Bypass Capacitor	284
7.3.2	Imperfect Grounding	286
7.3.3	Improper Connection	288
7.4	'Zero' Capacitor	290
7.4.1	What is a Zero Capacitor	290
7.4.2	Selection of a Zero Capacitor	290
7.4.3	Bandwidth of a Zero Capacitor	293
7.4.4	Combined Effect of Multi-Zero Capacitors	295
7.4.5	Chip Inductor is a Good Assistant	296
7.4.6	Zero Capacitor in RFIC Design	298
7.5	Quarter Wavelength of Microstrip Line	300
7.5.1	A Runner is a Part in RF Circuitry	300
7.5.2	Why Quarter Wavelength is so Important	304
7.5.3	Magic Open-Circuited Quarter Wavelength of Microstrip Line	305
7.5.4	Testing for Width of Microstrip Line with Specific Characteristic Impedance	307
7.5.5	Testing for Quarter Wavelength	307
	Appendices	309
7.A.1	Characterizing of Chip Capacitor and Chip Inductor by Means of $S_{21}$ Testing	309
7.A.2	Characterizing of Chip Resistor by Means of $S_{11}$ of $S_{22}$ Testing	319

Reference	321
Further Reading	322
Exercises	322
Answers	323

## **8 EQUIPOTENTIALITY AND CURRENT COUPLING ON THE GROUND SURFACE 325**

8.1	Equipotentiality on the Ground Surface	325
8.1.1	Equipotentiality on the Grounded Surface of an RF Cable	325
8.1.2	Equipotentiality on the Grounded Surface of a PCB	326
8.1.3	Possible Problems of a Large Test PCB	327
8.1.4	Coercing Grounding	328
8.1.5	Testing for Equipotentiality	333
8.2	Forward and Return Current Coupling	335
8.2.1	Indifferent Assumption and Great Ignore	335
8.2.2	Reduction of Current Coupling on a PCB	336
8.2.3	Reduction of Current Coupling in an IC Die	338
8.2.4	Reduction of Current Coupling between Multiple RF Blocks	340
8.2.5	A Plausible System Assembly	341
8.3	PCB or IC Chip with Multimetallic Layers	344
	Further Reading	346
	Exercises	346
	Answers	347

## **9 LAYOUT 349**

9.1	Difference in Layout between an Individual Block and a System	349
9.2	Primary Considerations of a PCB	350
9.2.1	Types of PCBs	350
9.2.2	Main Electromagnetic Parameters	351
9.2.3	Size	351
9.2.4	Number of Metallic Layers	352
9.3	Layout of a PCB for Testing	352
9.4	VIA Modeling	355
9.4.1	Single Via	355
9.4.2	Multivias	359
9.5	Runner	360
9.5.1	When a Runner is Connected with the Load in Series	360
9.5.2	When a Runner is Connected to the Load in Parallel	363
9.5.3	Style of Runner	363
9.6	Parts	369
9.6.1	Device	369
9.6.2	Inductor	369
9.6.3	Resistor	370
9.6.4	Capacitor	370
9.7	Free Space	371

References	373
Further Reading	373
Exercises	373
Answers	374

## **10 MANUFACTURABILITY OF PRODUCT DESIGN 377**

10.1 Introduction	377
10.2 Implication of $6\sigma$ Design	379
10.2.1 $6\sigma$ and Yield Rate	379
10.2.2 $6\sigma$ Design for a Circuit Block	382
10.2.3 $6\sigma$ Design for a Circuit System	383
10.3 Approaching $6\sigma$ Design	383
10.3.1 By Changing of Parts' $\sigma$ Value	383
10.3.2 By Replacing Single Part with Multiple Parts	385
10.4 Monte Carlo Analysis	386
10.4.1 A Band-Pass Filter	386
10.4.2 Simulation with Monte Carlo Analysis	387
10.4.3 Sensitivity of Parts on the Parameter of Performance	392
Appendices	392
10.A.1 Fundamentals of Random Process	392
10.A.2 Index $C_p$ and $C_{pk}$ Applied in $6\sigma$ Design	398
10.A.3 Table of the Normal Distribution	398
Further Reading	398
Exercises	399
Answers	399

## **11 RFIC (RADIO FREQUENCY INTEGRATED CIRCUIT) 401**

11.1 Interference and Isolation	401
11.1.1 Existence of Interference in Circuitry	401
11.1.2 Definition and Measurement of Isolation	402
11.1.3 Main Path of Interference in a RF Module	403
11.1.4 Main Path of Interference in an IC Die	403
11.2 Shielding for an RF Module by a Metallic Shielding Box	403
11.3 Strong Desirability to Develop RFIC	405
11.4 Interference going along IC Substrate Path	406
11.4.1 Experiment	406
11.4.2 Trench	408
11.4.3 Guard Ring	409
11.5 Solution for Interference Coming from Sky	411
11.6 Common Grounding Rules for RF Module and RFIC Design	412
11.6.1 Grounding of Circuit Branches or Blocks in Parallel	412
11.6.2 DC Power Supply to Circuit Branches or Blocks in Parallel	413
11.7 Bottlenecks in RFIC Design	414
11.7.1 Low- $Q$ Inductor and Possible Solution	414
11.7.2 "Zero" Capacitor	419

11.7.3	Bonding Wire	419
11.7.4	Via	419
11.8	Calculating of Quarter Wavelength	420
	Reference	423
	Further Reading	423
	Exercises	424
	Answers	425

## **PART 2 RF SYSTEM 427**

### **12 MAIN PARAMETERS AND SYSTEM ANALYSIS IN RF CIRCUIT DESIGN 429**

12.1	Introduction	429
12.2	Power Gain	431
12.2.1	Basic Concept of Reflection Power Gain	431
12.2.2	Transducer Power Gain	434
12.2.3	Power Gain in a Unilateral Case	437
12.2.4	Power Gain in a Unilateral and Impedance-Matched Case	438
12.2.5	Power Gain and Voltage Gain	439
12.2.6	Cascaded Equations of Power Gain	439
12.3	Noise	441
12.3.1	Significance of Noise Figure	441
12.3.2	Noise Figure in a Noisy Two-Port RF Block	443
12.3.3	Notes on Noise Figure Testing	444
12.3.4	An Experimental Method to Obtain Noise Parameters	445
12.3.5	Cascaded Equations of Noise Figure	446
12.3.6	Sensitivity of a Receiver	448
12.4	Nonlinearity	453
12.4.1	Nonlinearity of a Device	453
12.4.2	IP (Intercept Point) and IMR (Intermodulation Rejection)	461
12.4.3	Cascaded Equations of Intercept Point	472
12.4.4	Nonlinearity and Distortion	479
12.5	Other Parameters	480
12.5.1	Power Supply Voltage and Current Drain	480
12.5.2	Part Count	482
12.6	Example of RF System Analysis	482
	Appendices	485
12.A.1	Conversion between Watts, Volts, and $\text{dB}_m$ in a System with $50\ \Omega$ Input and Output Impedance	485
12.A.2	Relationship between voltage reflection coefficient, $\Gamma$ , and Transmission coefficients when the load $R_0$ is equal to the standard characteristic resistance, $50\ \Omega$ )	485
12.A.3	Definition of Powers in a Two-Port Block by Signal Flow Graph	488
12.A.4	Main Noise Sources	489



## CONTENTS

References	491
Further Reading	491
Exercises	493
Answers	494
<b>13 SPECIALITY OF "ZERO IF" SYSTEM</b>	<b>501</b>
13.1 Why Differential Pair?	501
13.1.1 Superficial Difference between Single-Ended and Differential Pair	501
13.1.2 Nonlinearity in Single-Ended Stage	503
13.1.3 Nonlinearity in a Differential Pair	505
13.1.4 Importance of Differential Configuration in a Direct Conversion or Zero IF Communication System	507
13.1.5 Why Direct Conversion or Zero IF?	508
13.2 Can DC Offset be Blocked out by a Capacitor?	508
13.3 Chopping Mixer	511
13.4 DC Offset Cancellation by Calibration	516
13.5 Remark on DC Offset Cancellation	517
Further Reading	517
Exercises	518
Answers	519
<b>14 DIFFERENTIAL PAIRS</b>	<b>521</b>
14.1 Fundamentals of Differential Pairs	521
14.1.1 Topology and Definition of a Differential Pair	521
14.1.2 Transfer Characteristic of a Bipolar Differential Pair	524
14.1.3 Small Signal Approximation of a Bipolar Differential Pair	527
14.1.4 Transfer Characteristic of a MOSFET Differential Pair	528
14.1.5 Small Signal Approximation of a MOSFET Differential Pair	530
14.1.6 What Happens If Input Signal Is Imperfect Differential	531
14.2 CMRR (Common Mode Rejection Ratio)	533
14.2.1 Expression of CMRR	533
14.2.2 CMRR in a Single-Ended Stage	539
14.2.3 CMRR in a Pseudo-Differential Pair	539
14.2.4 Enhancement of CMRR	541
Reference	542
Further Reading	542
Exercises	542
Answers	543
<b>15 RF BALUN</b>	<b>547</b>
15.1 Introduction	547
15.2 Transformer Balun	549

15.2.1	Transformer Balun in RF Circuit Design with Discrete Parts	550
15.2.2	Transformer Balun in RFIC Design	550
15.2.3	An Ideal Transformer Balun for Simulation	551
15.2.4	Equivalence of Parts between Single-Ended and Differential Pair in Respect to an Ideal Transformer Balun	555
15.2.5	Impedance Matching for Differential Pair by means of Transformer Balun	568
15.3	LC Balun	571
15.3.1	Simplicity of LC Balun Design	572
15.3.2	Performance of a Simple LC Balun	572
15.3.3	A Practical LC Balun	576
15.4	Microstrip Line Balun	580
15.4.1	Ring Balun	580
15.4.2	Split Ring Balun	582
15.5	Mixing Type of Balun	583
15.5.1	Balun Built by Microstrip Line and Chip Capacitor	583
15.5.2	Balun Built by Chip Inductors and Chip Capacitors	585
Appendices		586
15.A.1	Transformer Balun Built by Two Stacked Transformers	586
15.A.2	Analysis of a Simple LC Balun	588
15.A.3	Example of Calculating of $L$ and $C$ Values for a Simple LC Balun	592
15.A.4	Equivalence of Parts between Single-Ended and Differential Pair with Respect to a Simple LC Balun	592
15.A.5	Some Useful Couplers	602
15.A.6	Cable Balun	603
Reference		604
Further Reading		604
Exercises		605
Answers		606

<b>16</b>	<b>SOC (SYSTEM-ON-A-CHIP) AND NEXT</b>	<b>611</b>
16.1	SOC	611
16.1.1	Basic Concept	611
16.1.2	Remove Bottlenecks in Approach to RFIC	612
16.1.3	Study Isolation between RFIC, Digital IC, and Analog IC	612
16.2	What is Next	612
Appendices		615
16.A.1	Packaging	615
References		621
Further Reading		622
Exercises		622
Answers		623

**PART 3 INDIVIDUAL RF BLOCKS 625**

**17 LNA (LOW-NOISE AMPLIFIER) 627**

- 17.1 Introduction 627
- 17.2 Single-Ended Single Device LNA 628
  - 17.2.1 Size of Device 629
  - 17.2.2 Raw Device Setup and Testing 632
  - 17.2.3 Challenge for a Good LNA Design 639
  - 17.2.4 Input and Output Impedance Matching 646
  - 17.2.5 Gain Circles and Noise Figure Circles 648
  - 17.2.6 Stability 649
  - 17.2.7 Nonlinearity 653
  - 17.2.8 Design Procedures 655
  - 17.2.9 Other Examples 656
- 17.3 Single-Ended Cascode LNA 662
  - 17.3.1 Bipolar CE–CB Cascode Voltage Amplifier 662
  - 17.3.2 MOSFET CS–CG Cascode Voltage Amplifier 666
  - 17.3.3 Why Cascode? 669
  - 17.3.4 Example 671
- 17.4 LNA with AGC (Automatic Gain Control) 684
  - 17.4.1 AGC Operation 684
  - 17.4.2 Traditional LNA with AGC 686
  - 17.4.3 Increase in AGC Dynamic Range 688
  - 17.4.4 Example 689
- References 690
- Further Reading 690
- Exercises 691
- Answers 692

**18 MIXER 695**

- 18.1 Introduction 695
- 18.2 Passive Mixer 698
  - 18.2.1 Simplest Passive Mixer 698
  - 18.2.2 Double-Balanced Quad-Diode Mixer 699
  - 18.2.3 Double-Balanced Resistive Mixer 702
- 18.3 Active Mixer 706
  - 18.3.1 Single-End Single Device Active Mixer 706
  - 18.3.2 Gilbert Cell 708
  - 18.3.3 Active Mixer with Bipolar Gilbert Cell 712
  - 18.3.4 Active Mixer with MOSFET Gilbert Cell 715
- 18.4 Design Schemes 717
  - 18.4.1 Impedance Measuring and Matching 717
  - 18.4.2 Current Bleeding 718
  - 18.4.3 Multi-tanh Technique 719

18.4.4	Input Types	722
Appendices		723
18.A.1	Trigonometric and Hyperbolic Functions	723
18.A.2	Implementation of $\tanh^{-1}$ Block	724
References		726
Further Reading		726
Exercises		726
Answers		727
<b>19</b>	<b>TUNABLE FILTER</b>	<b>731</b>
19.1	Tunable Filter in A Communication System	731
19.1.1	Expected Constant Bandwidth of a Tunable Filter	732
19.1.2	Variation of Bandwidth	732
19.2	Coupling between two Tank Circuits	733
19.2.1	Inappropriate Coupling	735
19.2.2	Reasonable Coupling	738
19.3	Circuit Description	738
19.4	Effect of Second Coupling	739
19.5	Performance	743
Further Reading		746
Exercises		747
Answers		747
<b>20</b>	<b>VCO (VOLTAGE-CONTROLLED OSCILLATOR)</b>	<b>749</b>
20.1	“Three-Point” Types of Oscillator	749
20.1.1	Hartley Oscillator	751
20.1.2	Colpitts Oscillator	753
20.1.3	Clapp Oscillator	753
20.2	Other Single-Ended Oscillators	755
20.2.1	Phase-Shift Oscillator	755
20.2.2	TITO (Tuned Input and Tuned Output) Oscillator	757
20.2.3	Resonant Oscillator	757
20.2.4	Crystal Oscillator	758
20.3	VCO and PLL (Phase Lock Loop)	759
20.3.1	Implication of VCO	759
20.3.2	Transfer Function of PLL	760
20.3.3	White Noise from the Input of the PLL	763
20.3.4	Phase Noise from a VCO	764
20.4	Design Example of a Single-Ended VCO	769
20.4.1	Single-Ended VCO with Clapp Configuration	769
20.4.2	Varactor	770
20.4.3	Printed Inductor	770
20.4.4	Simulation	773
20.4.5	Load-Pulling Test and VCO Buffer	776
20.5	Differential VCO and Quad-Phases VCO	778

## CONTENTS

Reference	783
Further Reading	783
Exercises	784
Answers	784
<b>21 PA (POWER AMPLIFIER)</b>	<b>789</b>
21.1 Classification of PA	789
21.1.1 Class A Power Amplifier	790
21.1.2 Class B Power Amplifier	790
21.1.3 Class C Power Amplifier	791
21.1.4 Class D Power Amplifier	791
21.1.5 Class E Power Amplifier	792
21.1.6 Third-Harmonic-Peaking Class F Power Amplifier	793
21.1.7 Class S Power Amplifier	794
21.2 Single-Ended PA	794
21.2.1 Tuning on the Bench	795
21.2.2 Simulation	796
21.3 Single-Ended PA IC Design	798
21.4 Push–Pull PA Design	799
21.4.1 Main Specification	799
21.4.2 Block Diagram	799
21.4.3 Impedance Matching	800
21.4.4 Reducing the Block Size	804
21.4.5 Double Microstrip Line Balun	808
21.4.6 Toroidal RF Transformer Balun	817
21.5 PA with Temperature Compensation	822
21.6 PA with Output Power Control	823
21.7 Linear PA	824
References	828
Further Reading	828
Exercises	829
Answers	829