

Contents

Contributors	xv
Preface	xvii
Acknowledgments	xxi
1 Significance of Power Integrity for Integrated Circuits <i>Raj Nair and Masanori Hashimoto</i>	1
1.1 Transistor Scaling and PI Degradation Progression	2
1.1.1 PI under Constant-Power and Constant-Power-Density Scaling	4
1.1.2 Low-Power Design and PI Degradation	6
1.1.3 Power Grid Noise in ICs	7
1.1.4 Impact of PI Degradation on I/O Circuits and Signal Integrity	11
1.2 Implications of Worsening PI	13
1.2.1 Yield Spreading and Loss Through PI Degradation	13
1.2.2 Diminished Voltage Scaling and Increasing Power	15
1.2.3 Fabrication and Packaging Technology Enhancement and Cost	17
1.2.4 Design and Verification Cost	18
1.2.5 Unsustainable Energy Wastage	19
1.3 References	20
2 Supply and Substrate Noise Impact on Circuits <i>Masanori Hashimoto</i>	21
2.1 Supply Noise and Substrate Noise	22
2.2 Path and Cell Delays and Supply Noise	24
2.2.1 Relation between Path Delay and Supply Noise	25
2.2.2 Combinatorial Cell Delay	30
2.2.3 Flip-Flop Timing Characteristics	33
2.3 Noise-Aware Circuit-Level Timing Analysis	37
2.3.1 Difficulties	37
2.3.2 Spatial and Temporal Correlation of Supply Noise	40
2.3.3 Statistical Noise Modeling	44
2.3.4 A Case Study	46

2.4	Noise Impact on Analog/ <i>RF</i> Circuits	50
2.4.1	Supply Noise	50
2.4.2	Substrate Noise	52
2.5	Exercises	53
2.6	References	53
3	Clock Generation and Distribution with Power Integrity <i>Yasuhiro Ogasahara, Masanori Hashimoto, and Raj Nair</i>	55
3.1	Delay, Skew, and Jitter of the Clock	56
3.2	Interconnect Elements for a Clock Tree	59
3.2.1	Parasitic Components of Interconnect Elements	59
3.2.2	Definitions of Inductance	60
3.2.3	Inductance Extraction	61
3.2.4	Interconnect Simulation	68
3.2.5	Specifying Inductive Interconnect Elements	71
3.2.6	Signal Transition Time and Inductance	74
3.3	Clock Tree Structures and Simulation	76
3.3.1	Clock Tree Structure	76
3.3.2	Industrial CDN Implementations	79
3.4	Clock Skew Under Power Supply Noise	80
3.4.1	Power Supply Noise in Sequential Circuits	80
3.4.2	Noise-Aware CDN Simulation	82
3.4.3	A Case Study on Clock Skew Analysis under <i>V</i> and <i>T</i> Variation	83
3.4.4	Related Works on Clock Skew and Supply Noise	88
3.5	Clock Generation	89
3.5.1	Brief Discussion on PLLs and DLLs Relating to PI	90
3.5.2	PLL Architecture	91
3.5.3	Rule 1: Isolate PLL Circuits from Noise	93
3.5.4	Rule 2: Design Single-Ended Circuits and Physical Layout Differentially	95
3.5.5	Rule 3: Design Loop Filter, Bias Generator, and VCO PSRR and Noise	98
3.6	Clock Extraction for Data Communications	100
3.6.1	Bang-Bang Phase Detectors	101
3.6.2	Data Recovery DLLs and Phase Interpolators	101

3.7	Summary	101
3.8	References	102
4	Signal and Power Integrity Design for I/O Circuits <i>Toshio Sudo</i>	105
4.1	Introduction	105
4.2	Single-Ended I/O Design	106
4.2.1	Modeling Simultaneous Switching Output Noise	106
4.2.2	Measurement of SSO Noise and Correlation with Simulation	109
4.2.3	Measurement of On-Die PDN and Anti-resonance Peak in the Full PDN ...	112
4.2.4	Co-simulation of SI and PI	114
4.2.5	Synthesized Total PDN Impedance Seen from the ASIC Chip	118
4.2.6	Frequency-Dependent Target Impedance	121
4.2.7	Signal Degradation Estimation Employing Frequency-Dependent Target Impedance	123
4.3	Differential I/O Design	123
4.3.1	Modeling of Signal Integrity of Differential I/O Circuit	124
4.3.2	Differential Transmission Line, Influence of Crosstalk Noise and Through-Hole Stub	125
4.3.3	Common-Mode Conversion by Woven Fiberglass	128
4.4	Power Integrity Design and Evaluation in 3D System-in-Package (SiP)	131
4.4.1	Benefits of Wide Bus Structures	131
4.4.2	Three Stacked Chips and Configuration of 3D SiP	132
4.4.3	Total PDN Impedance and Impact on SSO Noise	136
4.5	Summary	142
4.6	References	145
5	Power Integrity Degradation and Modeling <i>Chung-Kuan Cheng, Xiang Hu, and Amirali Shayan</i>	147
5.1	Background	147
5.2	Power Integrity Modeling	150
5.2.1	Board Power Integrity	150
5.2.2	Package Power Integrity	151
5.2.3	On-Die Grid Power Integrity	151

5.3	Power Integrity Analysis	152
5.4	Frequency-Domain Analysis	152
5.5	Time-Domain Analysis	156
5.6	Target Impedance Background	156
5.7	Problem Formulation	157
5.8	Worst-Case PDN Output Voltage Noise	158
5.9	Impedance without Realizability Constraints	159
5.10	Impedance with Realizability Constraints	161
5.10.1	First-Order Impedance	161
5.10.2	Second-Order Impedance	162
5.11	Real Power Distribution Networks	169
5.11.1	Ideal LC Tank without ESR _c	169
5.11.2	Standard LC Tank with ESR _c	171
5.11.3	A Complete PDN Path	175
5.12	Summary	178
5.13	References	178
6	Lumped, Distributed, and 3D Modeling for Power Integrity <i>Chung-Kuan Cheng, Xiang Hu, and Amirali Shayan</i>	181
6.1	3D PDN Modeling	181
6.1.1	Distributed Power Grid Model	182
6.1.2	Current Stimulus Model	183
6.1.3	Lumped Model	184
6.1.4	Effect of On-Chip Inductance	186
6.2	3D PDN Analysis Flow	189
6.3	Experimental Results	190
6.3.1	Current Distribution Model	191
6.3.2	Resonance Phenomena	196
6.3.3	Decoupling Capacitance	203
6.3.4	Connection Impedance between Tiers	205
6.3.5	Worst-Case Voltage Noise	208
6.3.6	Rogue Wave	211
6.4	Summary	212
6.5	Exercises	213
6.6	References	215
7	Chip Temperature and PI impact <i>Kian Haghdad and Mohab Anis</i>	217
7.1	High-Temperature Effect on VLSI Circuits and Systems	217
7.1.1	Impact on Power	217
7.1.2	Implication for Performance	223
7.1.3	Reliability Concerns	228

7.2	Temperature Distribution and Impact on Voltage Drop	230
7.2.1	Distribution and Management of Temperature	230
7.2.2	Effect of Load Changes on Voltage Drop	234
7.2.3	Impact of Interconnect Resistance on Voltage Drop	235
7.3	Temperature and Voltage Drop Modeling and Estimation	236
7.3.1	Thermal Modeling	236
7.3.2	Direct Temperature Measurement	241
7.3.3	Modeling Voltage Drop	243
7.4	Thermal and Voltage Drop Profile for an Alpha Processor	244
7.5	Design Enhancements for Robust Power Distribution with High Temperature	250
7.5.1	Floor Planning	250
7.5.2	Supply Pad Assignment	252
7.5.3	From Design to Manufacturing	255
7.6	Summary	259
7.7	Exercises	260
7.8	References	262

8 Low-Power Techniques and PI Impact

	<i>Masanori Hashimoto and Raj Nair</i>	265
8.1	Power Dissipation of Digital CMOS Circuits and Voltage Scaling	265
8.1.1	Dynamic Power	266
8.1.2	Short-Circuit Power	266
8.1.3	Leakage Power	266
8.2	Voltage Scaling	267
8.3	Clock Gating	272
8.3.1	Overview	272
8.3.2	Power Integrity Issues	274
8.3.3	Charge Pump Active Noise Regulation	278
8.4	Power Gating	279
8.4.1	Overview	279
8.4.2	Inrush Current and Inrush Current-Induced Noise	280
8.4.3	Well Structure and Inrush Current-Induced Noise	283
8.4.4	Mitigating Inrush Current-Induced Noise	288

8.4.5	Decoupling	291
8.4.6	Architectural, System-Level Techniques and Active Noise Regulation	292
8.5	Exercises	296
8.6	References	296
9	Power Integrity Case Study Using the IBM POWER7+ Processor Chip <i>Howard H. Smith</i>	299
9.1	Introduction	299
9.2	IBM POWER7+ Description	300
9.3	Power Integrity Considerations for IBM Processor Chips	303
9.4	Load Current Estimation Approaches for Power Integrity	307
9.5	POWER7+ Power Grid Design Considerations	309
9.6	Static Power Grid Verification	317
9.7	Transient Power Grid Analysis	323
9.8	Acknowledgments	343
9.9	References	344
10	Carbon Nanotube Interconnect for Power Delivery <i>Navin Srivastava and Mizuhisa Nihei</i>	345
10.1	Why a New Interconnect Material?	346
10.1.1	Increasing Copper Interconnect Resistivity	346
10.1.2	Electromigration Reliability	347
10.1.3	Scaling Trends for Copper Interconnect Elements	348
10.2	Basic Properties of Carbon Nanotubes	349
10.2.1	Chirality	350
10.2.2	Current-Carrying Capacity	351
10.2.3	Thermal Conductivity	352
10.3	Electrical Properties of Carbon Nanotubes	352
10.3.1	Resistance	353
10.3.2	Capacitance	354
10.3.3	Inductance	355
10.4	Carbon Nanotube Interconnect Elements	356
10.4.1	Resistance of a Carbon Nanotube Interconnect	357
10.4.2	Capacitance of a Carbon Nanotube Interconnect	359
10.4.3	Inductance of a Carbon Nanotube Interconnect	361

10.5	Thermal Management with Carbon Nanotube Interconnect elements	361
10.5.1	Through-Silicon Vias for 3D ICs	362
10.6	Fabrication and Integration of CNT Interconnect Elements	364
10.6.1	Carbon Nanotube Integration with Standard VLSI Process	364
10.6.2	Salient Features of CNT Interconnect Fabrication	365
10.7	Carbon Nanotubes for Power Integrity	368
10.7.1	Structural and Thermal Benefits	368
10.7.2	Electromigration Reliability	369
10.7.3	Low-Resistance Power Grids	370
10.8	Summary	370
10.9	References	372
	Index	375