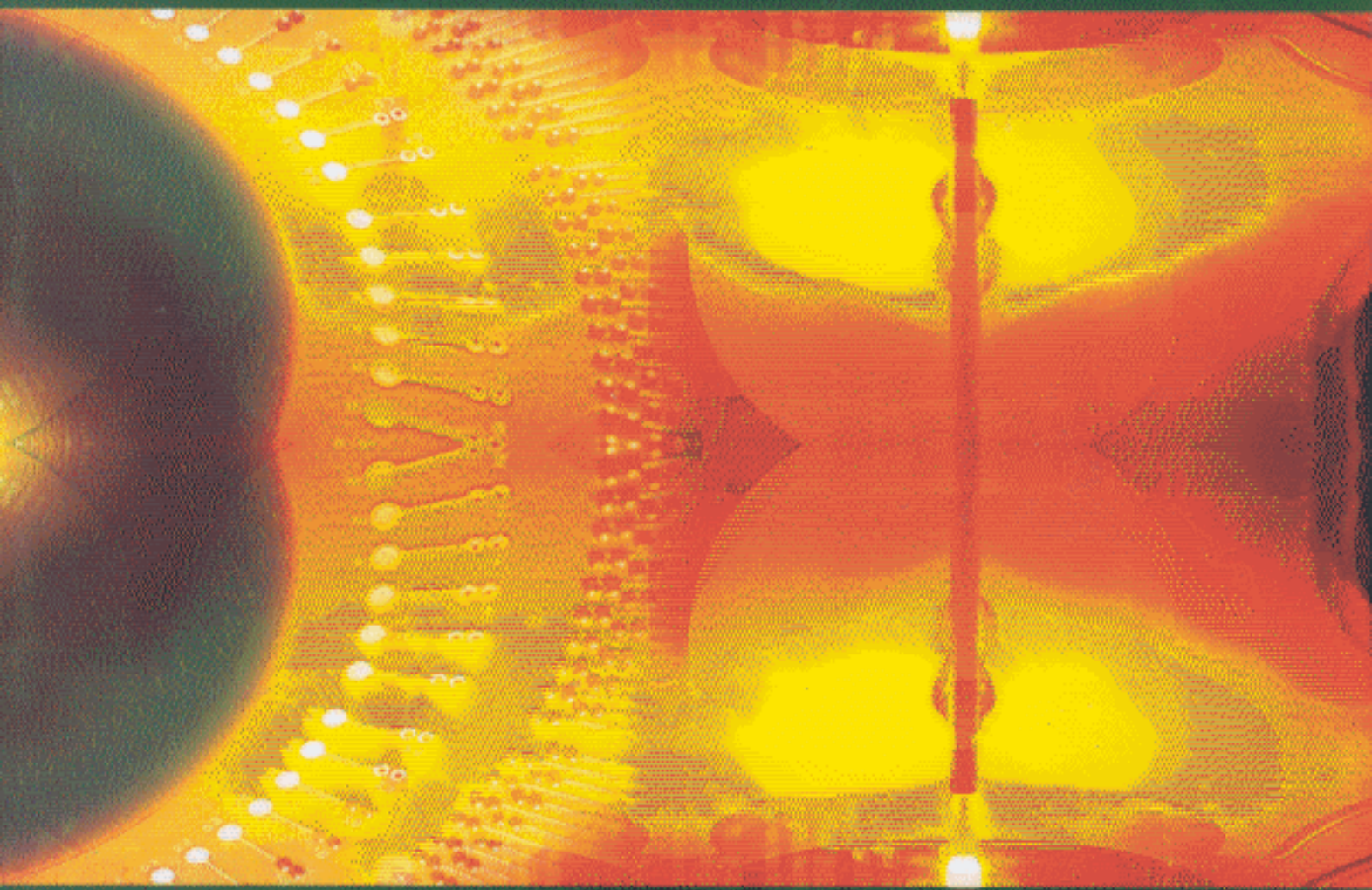
Digital Logic Simulation and CPLD Programming with VHDL



Steve Waterman

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Section 4: Appendices