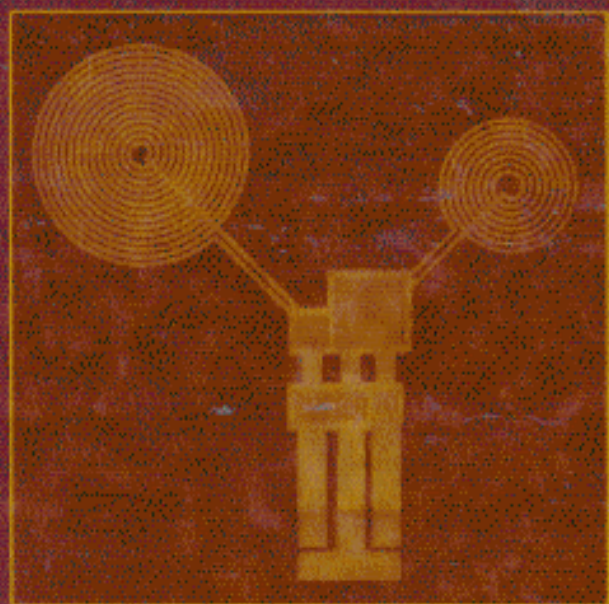


# Integrated Passive Component Technology



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# CONTENTS

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Contributors	xv
Preface	xvii
<b>1 Introduction</b>	<b>1</b>
<i>Richard K. Ulrich</i>	
1.1 Status and Trends in Discrete Passive Components	2
1.2 Definitions and Configurations of Integrated Passives	7
1.3 Comparison to Integrated Active Devices	10
1.4 Substrates and Interconnect Systems for Integrated Passives	11
1.4.1 Organic Substrates	12
1.4.2 Inorganic Substrates	14
1.5 Fabrication of Integrated Passives	14
1.6 Reasons for Integrating Passive Devices	17
1.7 Problems with Integrating Passive Devices	20
1.7.1 Cost Modeling	22
1.8 Applications for Integrated Passives	23
1.8.1 Replacing Surface Mount Discretes with Arrays and Networks	23
1.8.2 Decoupling	24
1.8.3 DC/DC Conversion	26
1.8.4 Passive Replacement in FR4	27
1.8.5 Passive Replacement in HDI	27
1.9 The Past and Future of Integrated Passives	27
1.10 Organization of this Book	29
References	30
<b>2 Characteristics and Performance of Planar Resistors</b>	<b>33</b>
<i>Richard K. Ulrich</i>	
2.1 Performance Parameters	33
2.1.1 Resistance of Planar Resistors	33
2.1.2 Resistivity of Materials	35

2.1.3	Temperature Effects	37
2.1.4	Value Stability	38
2.2	Resistance in Electronic Materials	40
2.2.1	Resistivity and Charge Carriers	40
2.2.2	Semiconducting Oxides	41
2.2.3	Tunneling	43
2.2.4	Temperature, Composition, and Morphology Effects	43
2.3	Sizing Integrated Resistors	45
2.3.1	Thermal Issues	46
2.3.2	Parasitic Capacitance between Meanders	49
2.3.3	Parasitic Capacitance to Ground	51
2.3.4	Lumped Versus Distributed Performance	52
2.4	Trimming	52
	References	53
<b>3</b>	<b>Integrated Resistor Materials and Processes</b>	<b>55</b>
	<i>Richard K. Ulrich</i>	
3.1	Single-Component Metals	56
3.2	Metal Alloys and Metal–Nonmetal Compounds	58
3.2.1	Tantalum Nitride	59
3.2.2	Titanium Oxy-Nitride	60
3.2.3	Nickel Phosphide	60
3.3	Semiconductors	61
3.3.1	Silicon	61
3.3.2	Semiconducting Oxides	61
3.4	Cermets	61
3.5	Polymer Thick Film	63
3.6	Ink Jet Deposition	65
3.7	Commercialized Processes	66
3.7.1	Ohmega-Ply®	66
3.7.2	Dupont Interra™	66
3.7.3	MacDermid M-Pass™	68
3.7.4	Polymer Thick Film	70
3.7.5	Shipley Insite™	70
3.8	Summary	70
	References	73
<b>4</b>	<b>Dielectric Materials for Integrated Capacitors</b>	<b>75</b>
	<i>Richard K. Ulrich</i>	
4.1	Polarizability and Capacitance	76
4.2	Capacitance Density	79
4.3	Temperature Effects	82
4.4	Frequency and Voltage Effects	83

4.5	Aging Effects	84
4.6	Composition and Morphology Effects	85
4.7	Leakage and Breakdown	86
4.8	Dissipation Factor	89
4.9	Comparison to EIA Dielectric Classifications	91
4.10	Matching Dielectric Materials to Applications	93
	4.10.1 Decoupling and Energy Storage	96
	4.10.2 Analog Functions	96
	4.10.3 Termination of Transmission Lines	96
	References	97
<b>5</b>	<b>Size and Configuration of Integrated Capacitors</b>	<b>101</b>
	<i>Richard K. Ulrich</i>	
5.1	Comparison of Integrated and Discrete Areas	101
5.2	Layout Options	105
5.3	Tolerance	106
5.4	Mixed Dielectric Strategies	107
5.5	CV Product	108
5.6	Maximum Capacitance Density and Breakdown Voltage	109
	References	111
<b>6</b>	<b>Processing Integrated Capacitors</b>	<b>113</b>
	<i>Richard K. Ulrich</i>	
6.1	Sputtering	114
6.2	CVD, PECVD and MOCVD	116
6.3	Anodization	117
	6.3.1 Benefits of Anodization for Capacitor Dielectrics	118
	6.3.2 Film Formation During Anodization	118
	6.3.3 Ta Anodization	120
	6.3.4 Dielectrics from Anodized Ta	121
	6.3.5 Patterning Ta and Ta <sub>2</sub> O <sub>5</sub>	123
	6.3.6 Ferroelectrics by Anodization	124
6.4	Sol-Gel and Hydrothermal Ferroelectrics	124
6.5	Thin- and Thick-Film Polymers	126
6.6	Thick-Film Dielectrics	127
	6.6.1 Ferroelectric Powder Dispersed in Polymer	127
6.7	Interlayer Insulation	129
6.8	Interdigitated Capacitors	130
6.9	Capacitor Plate Materials	131
6.10	Trimming Integrated Capacitors	131
6.11	Commercialized Integrated Capacitor Technologies	132
	6.11.1 DuPont Interra™	132
	6.11.2 3-M C-Ply	133

6.11.3	Dupont HK4	133
6.11.4	Motorola's Mezzanine Capacitor	135
6.11.5	Sanmina BC2000™	135
6.11.6	nChip	135
6.12	Summary	135
	References	138
<b>7</b>	<b>Defects and Yield Issues</b>	<b>145</b>
	<i>Richard K. Ulrich</i>	
7.1	Causes of Fatal Defects in Integrated Capacitors	145
7.2	Measurement of Defect Density	146
7.3	Defect Density and System Yield	147
7.3.1	Predicting Yield from Defect Density	148
7.4	Yield Enhancement Techniques for Capacitors	149
7.5	Conclusions	150
	References	151
<b>8</b>	<b>Electrical Performance of Integrated Capacitors</b>	<b>153</b>
	<i>Richard K. Ulrich and Leonard W. Schaper</i>	
8.1	Modeling Ideal Passives	154
8.2	Modeling Real Capacitors	154
8.3	Electrical Performance of Discrete and Integrated Capacitors	158
8.3.1	Inductance of the Capacitor Alone	158
8.3.2	Inductance of the Capacitor's Leads and Contacts	164
8.3.3	Equivalent Series Resistance	165
8.3.4	Capacitors as Distributed Devices	165
8.4	Dissipation Factor of Real Capacitors	166
8.5	Measurement of Capacitor Properties	166
8.5.1	ESR and ESL Measurement with an Impedance Analyzer	167
8.5.2	ESR and ESL Measurement with a Network Analyzer	170
8.6	Summary	174
	References	175
<b>9</b>	<b>Decoupling</b>	<b>177</b>
	<i>Leonard W. Schaper</i>	
9.1	Power Distribution	177
9.2	Decoupling with Discrete Capacitors	181
9.3	Decoupling with Integrated Capacitors	183
9.4	Dielectrics and Configurations for Integrated Decoupling	185
9.5	Integrated Decoupling as an Entry Application	187
	References	189

<b>10</b>	<b>Integrated Inductors</b>	<b>191</b>
	<i>Geert J. Carchon and Walter De Raedt</i>	
10.1	Introduction	191
10.2	Inductor Behavior and Performance Parameters	192
10.2.1	Inductor Layouts and Values	192
10.2.2	Inductor Operating Principles	194
10.2.3	Equivalent Circuit	196
10.2.4	Extraction of the Equivalent Circuit Parameters	198
10.2.5	Figure of Merits: $Q_L$ , $Q_{LC}$ , $FOM_L$	200
10.2.6	Spiral Inductor Layouts	206
10.2.7	Improving $Q_L$ by Technology and Layout Parameters	208
10.3	Inductor Performance Prediction	216
10.3.1	Transmission Line Inductor	217
10.3.2	Spiral Inductors	217
10.4	Integrated Inductor Examples	224
10.4.1	Inductors Integrated on 10–20 $\Omega$ -cm Si Substrates	224
10.4.2	GaAs MMIC Inductors	224
10.4.3	MCM-D Inductors	226
10.4.4	LTCC	230
10.4.5	Integration of On-Chip Si Inductors through Wafer-Level Packaging Techniques	231
10.5	Use of Inductors in Circuits: Examples	232
10.5.1	Filters	233
10.5.2	Voltage-Controlled Oscillators	235
10.5.3	Size-Reduction Techniques	235
10.5.4	Coupled Spiral Inductors	237
10.6	Conclusions	238
	Acknowledgments	238
	References	238
<b>11</b>	<b>Modeling of Integrated Inductors and Resistors for Microwave Applications</b>	<b>247</b>
	<i>Zhenwen Wang, M. Jamal Deen, and A. H. Rahal</i>	
11.1	Introduction	247
11.1.1	Miniature Hybrid Microwave Integrated Circuit (MHMIC)	248
11.1.2	Goals of this Chapter	248
11.2	Modeling of Spiral Inductors	249
11.2.1	Geometry of the Spiral Inductor	249
11.2.2	Inductor Circuit Model	250
11.2.3	Calculation of Inductance	250
11.2.4	Ground Plane Effect on Inductance	252
11.2.5	Series Resistance	253
11.2.6	Parasitic Capacitance	254

11.2.7	Summary of Spiral Inductor Model	257
11.2.8	Quality Factor of a Spiral Inductor	257
11.2.9	Inductor Synthesis	258
11.2.10	Design and De-Embedding of Inductor Test Structure	259
11.2.11	Measurement Setup and Calibration Specifications	261
11.2.12	Experimental Verification	261
11.2.13	Low-Pass Filter	263
11.2.14	Extension of the Model to Spiral Inductors on Silicon Substrates	265
11.3	Modeling of Thin-Film Resistors	271
11.3.1	Step Discontinuity in Microstrip Width	273
11.3.2	High Sheet Resistance Microstrip Model	274
11.3.3	Experimental Verification	278
11.3.4	S-parameter Measurement Setup	278
11.3.5	Measurement Calibration	278
11.4	Conclusions	282
	References	282
	Appendix: Characteristics of Microstrip Lines	284
A.1	Characteristic Impedance $Z_L$ and Effective Dielectric Constant $\epsilon_{\text{eff}}$ under Static TEM Approximation	234
A.2	Dispersion Models of Effective Dielectric Constant $\epsilon_{\text{eff}}$ and Characteristic Impedance $Z_L$	286
A.3	Lumped-Element Model of a Microstrip Line	288
A.4	Microstrip Losses	288
<b>12</b>	<b>Other Applications and Integration Technologies</b>	<b>293</b>
	<i>Elizabeth Logon, Geert J. Carchon, Walter De Raedt, Richard R. Ulrich, and Leonard W. Schaper</i>	
12.1	Demonstration Devices Fabricated with Integrated Passives	294
12.1.1	RC Terminators	294
12.1.2	Voltage Dividers	297
12.1.3	Reliability Test Structures	298
12.1.4	Filters and RF Devices	299
12.1.5	Functional Modules and Subsystems	305
12.2	Commercialized Thin-Film Build-Up Integrated Passives	313
12.2.1	Capacitor Arrays	314
12.2.2	Termination	315
12.2.3	Intarsia	316
12.2.4	SyChip	318
12.2.5	Telephus	320
12.3	Other Integrated Passive Technologies	320
12.4	Summary	322
	Acknowledgments	323
	References	323

<b>13 The Economics of Embedded Passives</b>	<b>327</b>
<i>Peter A. Sandborn</i>	
13.1 Introduction	327
13.2 Modeling Embedded Passive Economics	329
13.3 Key Aspects of Modeling Embedded Passive Costs	332
13.3.1 Board Size and Routing Calculations	332
13.3.2 Recurring Cost Analysis	336
13.3.3 Throughput	338
13.3.4 Trimming Embedded Resistors	341
13.3.5 Yield and Test	343
13.3.6 Life Cycle Costs	345
13.4 Example Case Studies	347
13.4.1 Picocell Board Application	348
13.4.2 NEMI Hand-Held Product Sector Emulator	352
13.4.3 Fiber Channel Card	354
13.5 Summary	356
Acknowledgments	357
References	357
<b>14 The Future of Integrated Passives</b>	<b>361</b>
<i>Richard K. Ulrich</i>	
14.1 Status of Passive Integration	361
14.2 Issues for Implementation on Organic Substrates	362
14.2.1 Electrical Design Issues	362
14.2.2 Board Design Issues	363
14.2.3 Fabrication and Manufacturing Issues	364
14.3 Progress on Board-Level Implementation	365
14.3.1 Advanced Embedded Passives Technology Consortium (AEPT)	366
14.3.2 National Electronics Manufacturing Initiative (NEMI)	366
14.3.3 The Embedded Capacitance Project	367
14.4 Three Ways In for Organic Boards	367
14.4.1 Decoupling	367
14.4.2 Replacement on FR4	369
14.4.3 High Density Interconnect	369
14.5 Conclusion	369
Index	373
About the Editors	