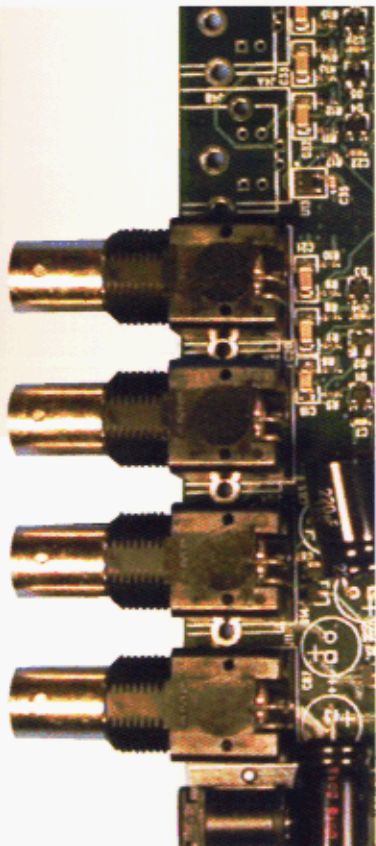
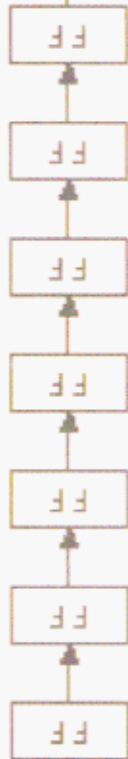




DIGITAL VIDEO ELECTRONICS

WITH 12 COMPLETE PROJECTS



Projects Include:
Multi-Image Processor, Scan Converter,
Image Scalar, Image Capture, Video Digitizer,
Digital Video Processor, CPLD Board, IR Link,
and much more



ANDREI CERNASOV

Contents

About the Author	x
Introduction	xi
Chapter 1. Human Vision	1
1.1 Fundamentals of Vision	1
1.2 Eye Anatomy	2
1.3 Spatial and Temporal Effects	5
1.3.1 Ricco's Law of Spatial Summation	5
1.3.2 Sensitivity versus Resolution	6
1.3.3 Bloch's Law of Temporal Summation	7
1.3.4 Weber's Law	7
1.3.5 The Broca-Sulzer Effect	8
1.3.6 Critical Flicker Frequency	8
1.3.7 The Ferry-Porter Law	8
1.3.8 The Brücke-Bartley Effect	9
Chapter 2. Video Signals and Standards	11
2.1 Designing Television	11
2.2 Analog Television Standards	12
2.3 Color Spaces	17
2.3.1 RGB	17
2.3.2 YCbCr	19
2.3.3 YPbPr	21
2.3.4 Gamma Correction	21
2.4 Sampling Formats	22
2.4.1 4:4:4	22
2.4.2 4:2:2	22
2.4.3 4:1:1	22
2.4.4 4:2:0	23

Contents

2.5	Introduction to Digital Video	24
2.5.1	Aspect Ratios	24
2.5.2	Why Digitize Video?	25
2.5.3	Digital Video Standards	26
2.5.3.1	SDTV 480i	27
2.5.3.2	SDTV 480p	28
2.5.3.3	SDTV 480i 16:9	29
2.5.3.4	HDTV 720p	29
2.5.3.5	HDTV 1080i	30
2.5.3.6	HDTV 1080p	32
2.5.3.7	HDTV RGB	32
2.5.4	Serial Digital Video—SDI and HD-SDI	33
2.5.5	SDTV and HDTV Voltage Levels	35
2.6	Special Video Connectors	35
Chapter 3.	Digital Video Applications	39
3.1	Image Capture Cards	39
3.2	Frame Synchronizer	41
3.3	Scan Converter/Video Scaler	42
3.4	Graphics, Logo, and Character Inserters	46
3.5	PIPs, SbSs, and PoPs with Genlock	48
3.6	QUAD Security Processor	49
3.7	Videophone	50
3.8	Videowall Controller	54
3.9	Video to LED Array Processor	54
3.10	Alpha Channel Mixer and Cross-Fader	58
3.11	Chroma Key Overlay	61
3.11.1	Simulated First Down Lines, Waving Pool Flags, and Ads	63
3.12	360-Degrees Omnivision	64
3.13	3-D Stereo Vision with Liquid Crystal Shutter Glasses	65
3.14	Telepresence Appliance for the Disabled	68
3.15	Dual Energy X-Ray Security Scanner	68
3.16	High-Resolution/High-Definition Processors	73
3.17	Portable Electronics	75
Chapter 4.	Working with Function Blocks	77
4.1	Requirements Specification Document	77
4.2	Functional Block Diagram	79
4.3	Selecting the Core Integrated Circuits	81
4.4	Matching the Blocks	83
4.4.1	Mixed Voltage Levels	85
4.4.2	Matching Bus Widths	87
4.4.3	Matching Data Speeds	89
4.5	Clock Generation	91
4.5.1	PLL with Integer Frequency Multiplier	92

4.5.2	PLL with Rational Frequency Multiplier	93
4.5.3	Clock Tree	93
4.6	Clock Distribution	95
4.6.1	Zero-Delay Clock Buffer	95
4.6.2	Clock Delay Equalizer Buffer	95
4.7	Multiple Voltage Power Supplies	96
4.7.1	Multiple Voltage Ladders	96
4.7.2	Mixed Voltage Supplies	96
4.7.3	Power Sequencing	98
 Chapter 5. Video Input and Output Circuits		 99
5.1	Video Transmission Lines	99
5.2	Input/Output ESD Circuit Protection	102
5.3	Analog Inputs and Outputs	107
5.3.1	Single-Sided Analog Drivers and Receivers	107
5.3.2	S-Video Drivers and Receivers	109
5.3.3	VGA, XGA, UXGA Video Drivers and Receivers	110
5.3.4	Opamp Differential Drivers	111
5.3.5	Opamp Differential Receivers	112
5.3.6	Twisted Pair Differential Link	112
5.4	Digital Inputs and Outputs	113
5.4.1	Digital Video Drivers	114
5.4.2	Digital Driver Circuit	114
5.4.3	Eye Pattern Test	115
5.4.4	Digital Receiver/Equalizer	116
5.4.5	Receiver/Equalizer Circuit	117
5.4.6	Clock and Data Recovery, Reclocking	118
5.4.7	Reclocker Circuit	119
5.5	LVDS Drivers and Receivers	119
 Chapter 6. Video Distribution		 125
6.1	Analog Distribution Amplifiers (DAs)	125
6.1.1	Composite DA	125
6.1.2	S-Video DA	125
6.1.3	VGA, XGA, UXGA DA	127
6.2	Analog Switches and Multiplexers	127
6.3	Analog Matrix Switches	127
6.3.1	Expanding Matrix Switches	130
6.3.2	Analog Matrix Switch Circuit	130
6.4	SDI, HD-SDI Distribution Amplifiers	132
6.4.1	SDI, HD-SDI 1 → 2 DA Circuit	132
6.5	SDI, HD-SDI Matrix Switches	134
6.5.1	SDI, HD-SDI 8 × 8 Matrix Switch Circuit	134
6.6	Parallel Digital Switches	136
6.6.1	Parallel Video—Background Color YCbCr Switch	137

Chapter 7. Controller Infrastructure	139
7.1 Controller Video IC Interfaces; I ² C, SPI	139
7.1.1 I ² C Bus	139
7.1.2 SPI Bus	142
7.2 System Controllers	143
7.2.1 Minimal Controller Circuit	145
7.2.2 Expanded Controller Circuit	146
7.3 System Resources	146
7.3.1 I ² C Controller	146
7.3.2 I ² C Repeater/Translator	149
7.3.3 Nonvolatile Memory (EEPROM)	149
7.3.4 Reset/Watchdog/Battery Backup	149
7.3.5 Real Time Clock (RTC)	150
7.3.6 Cooling Fan with Temperature Sensor	150
7.3.7 General Purpose Decoder and IO	151
7.4 Host and Slave Interfaces	151
7.4.1 RS-232/422/485 Driver Circuits	151
7.4.2 IrDA Interface and Controller Circuit	153
7.4.3 USB Interface and Controller Circuit	156
7.5 User Interface	162
7.5.1 Segment Displays	163
7.5.2 Matrix LED Displays	163
7.5.3 LCD Displays	163
7.5.4 Keypad Encoder	165
7.5.5 Tone/Tune Generator	165
Chapter 8. Video Decoders, Graphic Digitizers, and Deserializers	167
8.1 Theory of Signal Sampling	167
8.1.1 Frequency Spectrum of Sampled Signals	171
8.2 Front-End Functions	172
8.2.1 Anti-aliasing Filters for Composite, S-Video, RGB, and YPbPr	172
8.2.2 Automatic Gain Control	175
8.2.3 DC Restoration	176
8.2.4 Sync Signal Separation	178
8.2.4.1 Sync Separation Circuit with DC Restore	179
8.3 Video Decoder-Digitizer	179
8.3.1 Y/C Separation	181
8.3.2 Chroma Modulation and Demodulation	182
8.3.3 Contrast, Brightness, Saturation, and Hue	184
8.3.4 Video Decoder-Digitizer Circuit	186
8.4 Video Graphics Digitizers	191
8.4.1 Video Graphics Digitizer Circuit	192
8.4.2 VGA, XGA, UXGA Digitizer Circuit	194
8.4.3 HDTV Digitizer Circuit	196
8.5 Deserializing SDI Digital Video	197
8.5.1 Deserialzer Circuit	200

Chapter 9. Video Encoders, Graphics Digital to Analog Converters, and Serializers	205
9.1 Theory of Signal Reconstruction	205
9.1.1 Frequency Spectrum of Reconstructed Signals	207
9.2 Video Encoders	208
9.2.1 Video Encoder Circuit	209
9.3 Video Graphics DAC	212
9.3.1 Video Graphics DAC Circuit (VGA, XGA, SDTV, HDTV)	212
9.4 Serializing SDI Video	216
9.4.1 Serializer/Driver Circuit	219
Chapter 10. Video Memory	221
10.1 I/O Memory Buffers	221
10.1.1 Field Synchronization—Field Inversion	223
10.1.2 Frame Synchronization—Image Tear	225
10.1.3 Dual-Bank Full Frame Buffers	227
10.1.4 Single-Bank Full Frame Buffers	227
10.2 Memory Devices	227
10.2.1 Static RAM	229
10.2.1.1 Multi-Image Vertical Display with RAM Buffers	230
10.2.2 DRAM	235
10.2.3 SDRAM	237
10.2.4 FIFO DRAM	240
10.2.4.1 FIFO DRAM Circuit	241
10.2.5 FLASH Memory	243
Chapter 11. Combining Video Images	245
11.1 Overlay Processor	245
11.2 Raster Generation for Progressive Video	247
11.3 Raster Generation for Interlaced Video	249
11.4 Raster Generator Design for Interlaced Video	253
11.4.1 Interlaced Raster Generation Design Example	256
11.5 The Picture-in-Picture Overlay	260
11.5.1 Adding Borders	262
11.5.2 Adding Shadows	263
11.6 Graphics Key Overlay	266
11.6.1 Adding Transparency	268
11.7 Multiple Video Overlays	269
11.7.1 Design Definition	269
11.7.2 Overlay Processor	270
11.7.3 Multiple Video Overlays—Design Example	272
11.8 CPLD Circuit	288

Chapter 12. Image Scalers	289
12.1 Quick Theory of Digital Filters	289
12.1.1 The Laplace and Z-Transforms	289
12.1.2 Digital Filters	291
12.1.2.1 Transfer Function	291
12.1.2.2 Direct Recursive Realization	292
12.1.2.3 Canonic Recursive Realization	293
12.1.2.4 Cascade Realization	294
12.1.2.5 Parallel Realization	294
12.1.3 The Digital Comb Filter	295
12.2 Up-Sampling and Interpolation (Up-Scaling)	296
12.2.1 Spectrum of Up-Sampled Signals	298
12.2.2 Anti-Imaging Filters	298
12.3 Down-Sampling and Decimation (Down-Scaling)	299
12.3.1 Spectrum of Down-Sampled Signals	300
12.3.2 Anti-Aliasing Filters	301
12.4 Rational Number Sampling (Scaling)	302
12.5 Multirate Processing	302
12.5.1 Polyphase Decomposition	303
12.5.2 Polyphase Decimator	304
12.5.3 Polyphase Interpolator	306
12.6 Image Scalers	307
12.7 Commercial Image Scaler ICs	310
Chapter 13. Image Compression and Decompression	317
13.1 JPEG Compression and Decompression	317
13.1.1 Discrete Cosine Transform	317
13.1.2 Quantization Matrices	321
13.1.3 Zig-Zag Scanning	326
13.1.4 Huffman Coding	326
13.1.5 Run Length Encoding	329
13.2 MPEG Data Compression and Decompression	330
13.2.1 I, P, and B Frames	330
13.2.2 Motion Estimation	332
13.2.3 Frame Reordering	333
13.2.4 MPEG Data Hierarchy	334
13.3 MPEG Encoders (Coders) and Decoders	336
13.3.1 Scalable SNR Designs	337
13.3.2 Scalable Resolution Designs	339
13.4 MPEG Encoder Circuit	340
Chapter 14. PCB Layout of Video	345
14.1 Ground Bounce	345
14.2 Board Partitioning	347
14.3 Ground and Power Planes, Plane Stacking	349

14.4	Return Currents and Loops	353
14.5	Signal Traces	356
14.6	Line Terminators	359
14.7	Power Supply Filters and Decouplers	362
14.8	Component Selections	364

Chapter 15. Digital Video Projects **367**

15.1	Project 1—Video Encoder and Color Bar Generator	367
15.2	Project 2—General Purpose CPLD Processor Board	376
15.3	Project 3—Color Raster Generator	391
15.4	Project 4—Framed Box Raster Generator	397
15.5	Project 5—Video Decoder-Digitizer	409
15.6	Video Buffer Board with Memory FIFOs	415
15.7	Project 6—Digital Video Processor	418
15.8	Project 7—Simple Image Scaler	429
15.9	Project 8—Controller Board	434
15.10	Project 9—Image Capture Appliance	437
15.11	Project 10—Graphics Display Appliance	443
15.12	Project 11—Scan Converter	445
15.13	Project 12—Wire and Infrared (IR) Remote Control	445
15.14	Notes	457

Index	459
--------------	------------